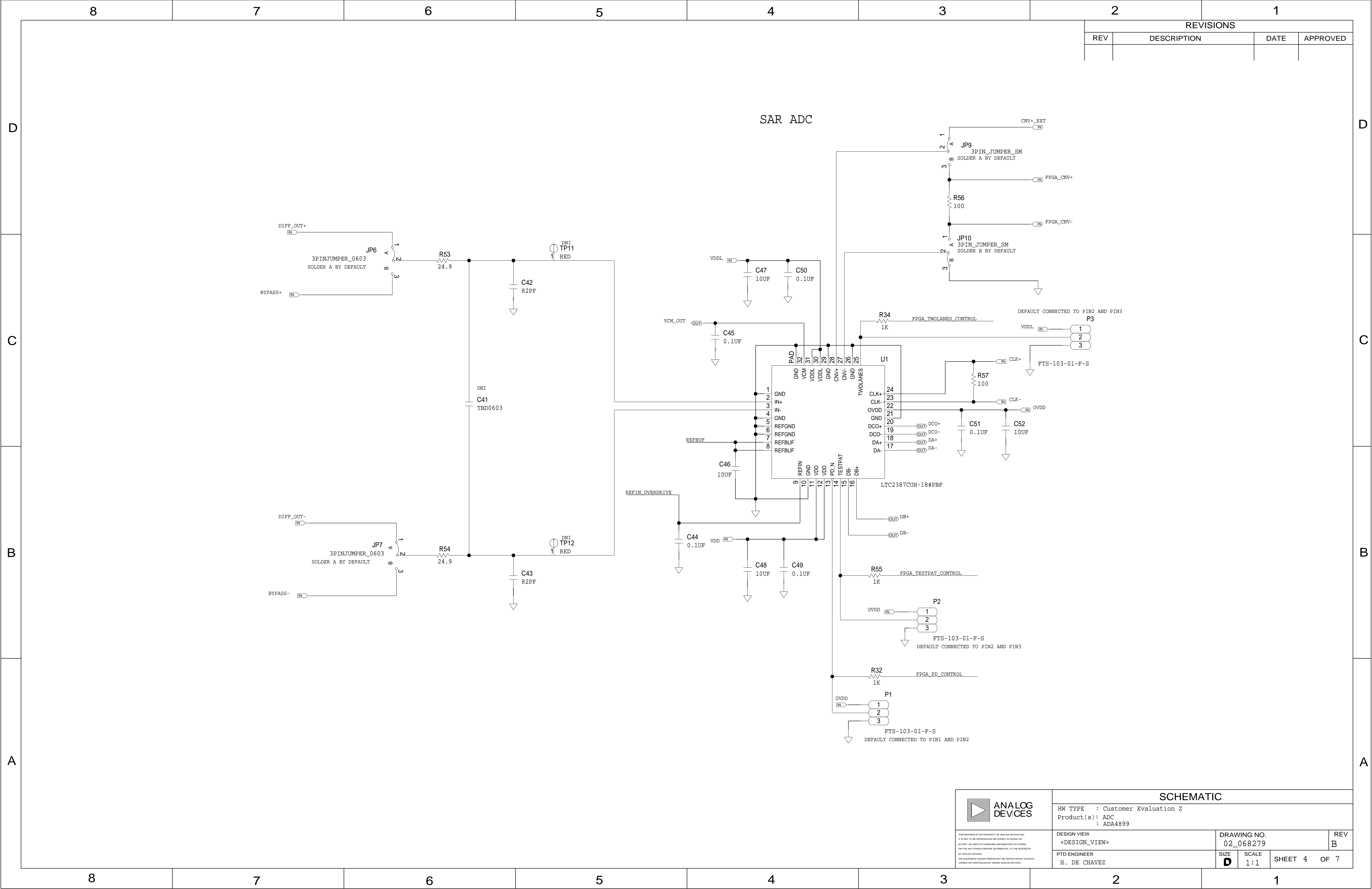


[illegible]



VDDL

IN

C47

10UF

C50

0.1UF

VCM_OUT

OUT

C45

0.1UF

REFBUF

C46

10UF

REFIN_OVERDRIVE

C44

0.1UF

VDD

IN

C48

10UF

C49

0.1UF

U1

LTC2387CUH-18#PBF

CLK+

24

CLK-

23

IN+

22

IN-

21

OVDD

20

GND

19

DCO+

18

DCO-

17

DA+

16

DA-

15

DB+

14

DB-

13

TESTPAT

12

PD_N

11

VDD

10

GND

9

REFIN

8

REFGND

7

REFGND

6

GND

5

IN+

4

IN-

3

GND

2

PAD

1

CONV+

28

CONV-

27

VDDL

26

GND

25

TWOLANES

24

CLK+

23

CLK-

22

IN+

21

IN-

20

OVDD

19

GND

18

DCO+

17

DCO-

16

DA+

15

DA-

14

DB+

13

DB-

12

TESTPAT

11

PD_N

10

VDD

9

GND

8

REFIN

7

REFGND

6

REFGND

5

GND

4

IN+

3

IN-

2

GND

1

R34

1K

FPGA_TWOLANES_CONTROL

CLK+

IN

R57

100

CLK-

IN

C51

0.1UF

C52

10UF

OVDD

IN

R32

1K

FPGA_PD_CONTROL

OVDD

IN

R55

1K

FPGA_TESTPAT_CONTROL

OVDD

IN

JP9

3PIN_JUMPER_SM

SOLDER A BY DEFAULT

CONV+_EXT

IN

FPGA_CONV+

IN

R56

100

FPGA_CONV-

IN

JP10

3PIN_JUMPER_SM

SOLDER B BY DEFAULT

P3

1

2

3

VDDL

IN

FTS-103-01-F-S

P2

1

2

3

OVDD

IN

FTS-103-01-F-S

P1

1

2

3

OVDD

IN

FTS-103-01-F-S

DEFAULT CONNECTED TO PIN1 AND PIN2

DEFAULT CONNECTED TO PIN2 AND PIN3

ANALOG

DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

HW TYPE : Customer Evaluation Z

Product(s): ADC

: ADA4899

DESIGN VIEW

<DESIGN_VIEW>

PTD ENGINEER

H. DE CHAVEZ

DRAWING NO.

02_068279

REV

B

SIZE

D

SCALE

1:1

SHEET

4

OF

7

